WHAT IS CLAIMED IS:

1. A clock recovery system comprising:

a CMU, generating a plurality of clock signals, the clock signals each approximate the same frequency and having differing phases;

a plurality of CRUs receiving the clock signals generated by the CMU and receiving at least one of a plurality of data signals;

a first mixer stage in each CRU receiving the clock signals generated by the CMU and mixing the clock signals generated by the CMU to form additional clock signals approximate the same frequency and having differing phases; and

a second mixer stage in each CRU receiving the additional clock signals and forming a recovered clock signal using at least some of the additional clock signals and a selection signal.

2. The clock recovery system of claim 1 wherein each CRU further comprises a phase detector which compares the recovered clock signal with at least one of the data signals.

3. The clock recovery system of claim 2 wherein the additional clock signals have finer phase differences than the clock signals generated by the CMU.

4. The clock recovery system of claim 3 wherein the phase detector generates at least one signal used in forming the selection signal.

5. The clock recovery system of claim 4 wherein the second mixer stage sums either complementary or non-complementary

versions of the additional clock signals to produce the recovered clock signal.

6. The clock recovery system of claim 5 wherein each CRU further comprises a low pass filter receiving the at least one signal generated by the phase detector, the low pass filter generating the selection signal.

7. A single chip clock recovery system comprising:

a single clock-generating unit, generating a plurality of clock signals;

a clock distribution network receiving the clock signals; and

a plurality of CRUs each receiving the clock signals from the clock distribution network and one of a plurality of data signals, each of the CRUs including:

a phase detector comparing the one of the data signals and a recovered clock signal formed by the CRU, the phase detector generating a phase difference signal;

a weighted mixer generating a plurality of further clock signals using the plurality of clock signals; and

a combiner selectively combining at least some of the plurality of further clock signals to form the recovered clock signal, the combiner using a selector signal based on the phase difference to selectively combine the further clock signals.

8. The single chip clock recovery system of claim 7 wherein the clock signals generated by the CMU have a substantially fixed phase difference.

9. The single chip data recovery system of claim 8 wherein each CRU includes a filter/accumulator receiving the phase difference signal.

10. A clock generation system comprising:

means for generating multiple out-of-phase clock signals, the clock signals being approximate a predetermined frequency;

means for producing a recovered clock signal, using at least two of the clock signals generated by the means for generating multiple out-of-phase clock signals, the recovered clock signal having a selectively variable phase and a frequency approximate the frequency of the multiple out of phase clock signals.

11. The clock generation system of claim 10 further comprising means for maintaining a specified phase of the recovered clock signal with respect to a received data signal.

12. The clock generation system of claim 10 wherein the means for producing a recovered clock signal includes means for mixing the at least two clock signals in varying amounts to form a plurality of intermediate clock signals with differing phases.

13. The clock generation system of claim 12 wherein the means for mixing the at least two clock signals includes multiple levels of mixing, each level of mixing generating a plurality of intermediate clock signals.

14. The clock generation system of claim 13 wherein the means for producing a recovered clock signal includes means for selecting at least one of the intermediate clock signals and

means for generating a recovered clock signal using the selected intermediate clock signals.